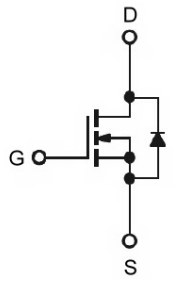
MSP100N055SA

N-Channel 100-V (D-S) MOSFET

Description

The device is using trench DMOS technology. This advanced technology has been especially tailored to minimize $R_{DS(ON)}$, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

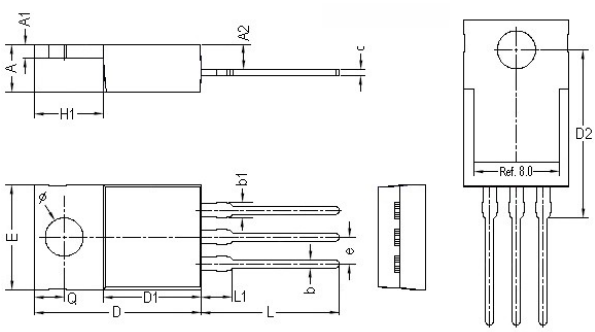
Graphic Symbol



Features

- $R_{DS(ON)}$ =5.5mΩ@ V_{GS} =10V
- Fast switching
- Improve dv/dt Capability
- 100% EAS Guaranteed
- Green Device Available

Package Dimension



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	4.30	4.70	D2	15.70	17.00
A1	1.20	1.40	E	9.70	10.36
A2	2.30	2.79	e	2.54 BSC	
b	0.70	0.90	H1	6.10	6.70
b1	1.20	1.75	L	12.80	13.90
c	0.34	0.60	L1	-	4.00
D	14.70	16.10	Q	2.60	3.00
D1	8.60	9.30	Ø	3.55	3.95

Typical Applications

- Motor Driver
- Load Switch
- Synchronous Rectifier
- BMS Applications

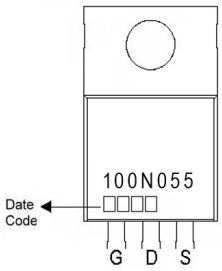
Package type：TO-220

Packing & Order Information

2,000/Box

RoHS Compliant

Marking



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MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings			
Symbol	**Parameter**	**Value**	**Units**
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	±20	V
I_D	Continuous Drain Current[1] (T_C =25°C)	120	A
	Continuous Drain Current[1] (T_C =100°C)	100	A
I_{DM}	Pulsed Drain Current[1,2]	480	A
I_{AS}	Single Pulse Avalanche Current, L =0.5mH[3]	53	A
E_{AS}	Single Pulse Avalanche Energy, L =0.5mH[3]	702	mJ
P_D	Power Dissipation[4] (T_C =25°C)	250	W
	Power Dissipation[4] (T_A =25°C)	2	W
T_J/T_{STG}	Operating Junction and Storage Temperature	-50 to +150	°C

Thermal Resistance Ratings			
Symbol	**Parameter**	**Maximum**	**Units**
$R_{\theta JA}$	Maximum Junction-to-Ambient[1]	62.5	°C/W
$R_{\theta JC}$	Maximum Junction-to-Case[1]	0.5	°C/W

Electrical Characteristics (T_J=25°C unless otherwise specified)						
Symbol	**Parameter**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Units**
$V_{GS\ (th)}$	Gate Threshold Voltage	V_{DS} =V_{GS}, I_D =250μA	2	3	4	V
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} =0V, I_D =250μA	100	-	-	V
g_{fs}	Forward Transconductance	V_{DS} =5V, I_D =30A	-	50	-	S
I_{GSS}	Gate-Source Leakage Current	V_{DS} =0V, V_{GS} =±20V	-	-	±100	nA
I_{DSS}	Drain-Source Leakage Current	V_{DS} =100V, V_{GS} =0V, T_J =25°C V_{DS} =100V, V_{GS} =0V, T_J =125°C	-	-	1 10	μA
$R_{DS\ (on)}$	Static Drain-Source On-Resistance[2]	V_{GS} =10V, I_D =30A	-	4.5	5.5	mΩ
EAS	Single Pulse Avalanche Energy[5]	V_{DD} =25V, L =0.5mH, I_{AS} =20A	100	-	-	mJ
V_{SD}	Diode Forward Voltage[2]	I_S =50A, V_{GS} =0V, T_J =25°C	-	-	1.3	V
I_S	Continuous Source Current[1,6]	V_G =V_D =0V, Force Current	-	-	120	A
I_{SM}	Pulsed Source Current[2,6]		-	-	240	

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Dynamic						
Symbol	**Parameter**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Units**
Q_g	Total Gate Charge[2]	V_{DS} =50V I_D =20A V_{GS} =10V	--	72	--	nC
Q_{gs}	Gate-Source Charge		--	28	--	
Q_{gd}	Gate-Drain Charge		--	15	--	
$t_{d(on)}$	Turn-On Delay Time[2]	V_{DD} =50V I_D =20A V_{GS} =10V R_G =3.0Ω	--	35	--	ns
t_r	Rise Time		--	18	--	
$t_{d(off)}$	Turn-Off Delay Time		--	45	--	
t_f	Fall Time		--	55	--	
C_{iss}	Input Capacitance	V_{DS} =50V V_{GS} =0V f =1.0MHz	--	4725	--	pF
C_{oss}	Output Capacitance		--	609	--	
C_{rss}	Reverse Transfer Capacitance		--	14	--	
Rg	Gate Resistance	V_{GS} =V_{DS} =0V, f =1.0MHz	--	1	--	Ω
trr	Reverse Recovery Time	I_F=30A, dI/dt=100A/μs, Tj=25°C		70		nS
Qrr	Reverse Recovery Charge			170		nC

Notes

1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%.
3. The EAS data shows maximum rating. The test condition is V_{DD}=25V, V_{GS}=10V, L=0.5mH, I_{AS}=53A.
4. The power dissipation is limited by 150℃ junction temperature.
5. The Min. value is 100% EAS tested guarantee.
6. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

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- **Typical Electrical Characteristics**

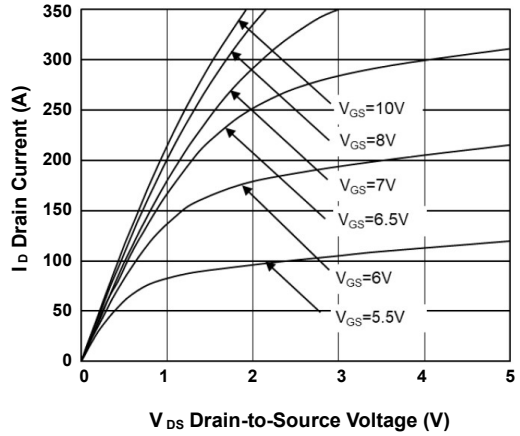

FIG.1-Typical Output Characteristics

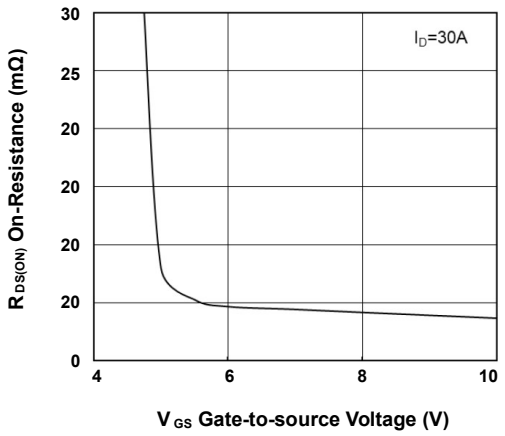

FIG.2-On-Resistance vs. G-S Voltage

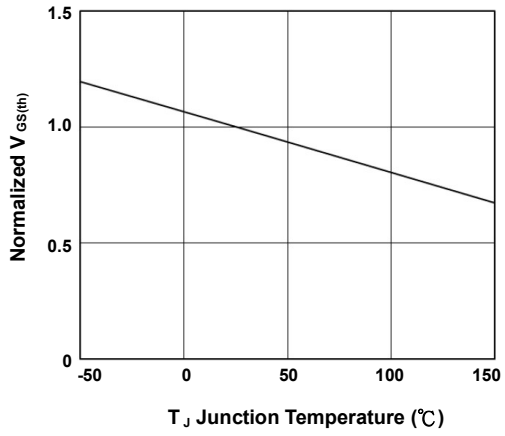

FIG.3-Normalized $V_{GS(th)}$ vs. T_J

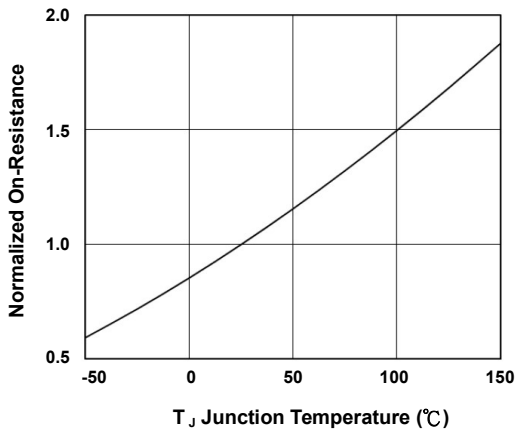

FIG.4-Normalized R_{DSON} vs. T_J

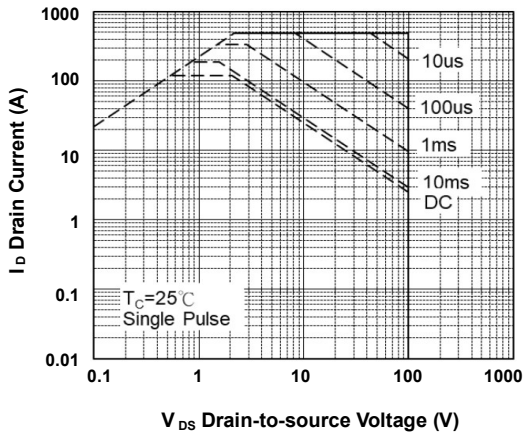

FIG.5-Safe Operating Area

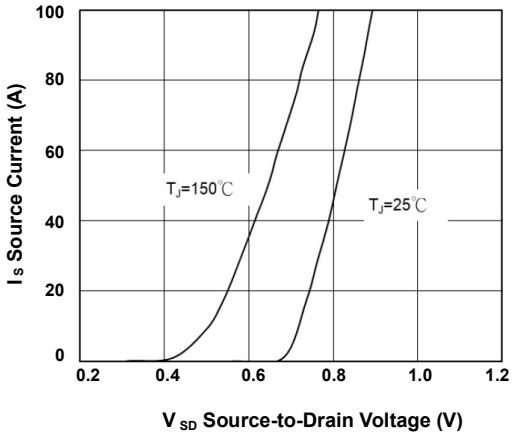

FIG.6-Source Drain Forward Characteristics

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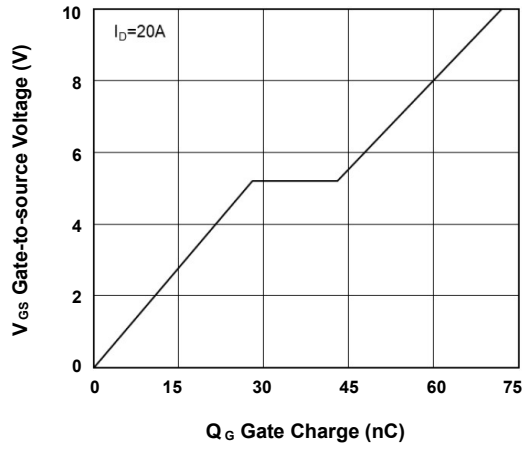

FIG.7-Gate Charge Characteristics

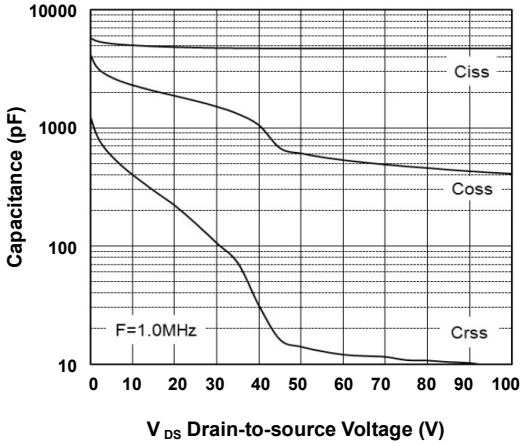

FIG.8-Capacitance Characteristics

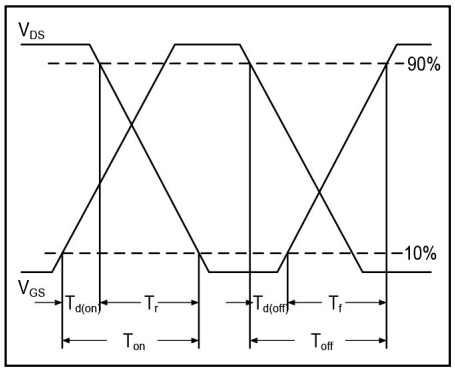

FIG.9-Switching Time Waveform

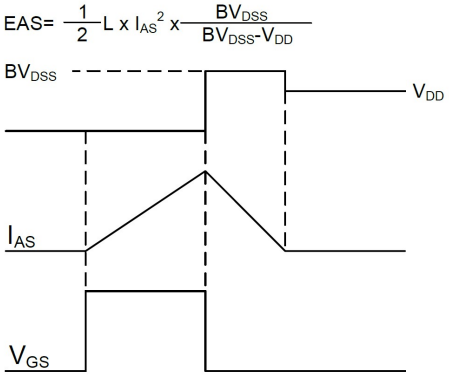

FIG.10-Unclamped Inductive Switching Waveform

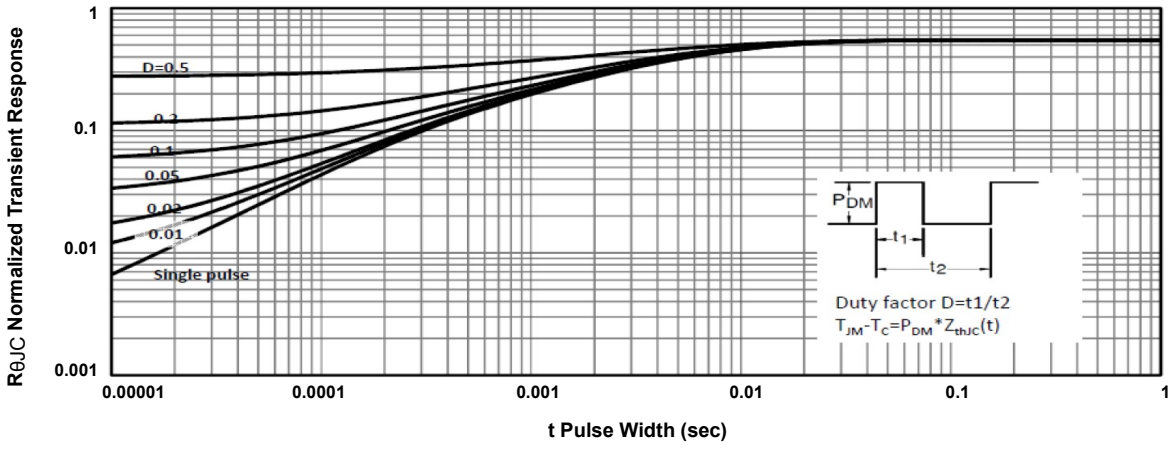

FIG.11-Normalized Maximum Transient Thermal Impedance

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