

# MSL60N04

## N-Channel 60-V (D-S) MOSFET

### Description

The MSL60N04 is the highest performance trench N-ch MOSFETs with extreme high cell density, which provide excellent  $R_{DS(ON)}$  and gate charge for most of the small power switching and load switch applications.

The device meets the RoHS and Green Product requirement with full function reliability approved.

### Features

- Advanced high cell density Trench technology
- Low On-Resistance
- Low Miller Charge
- Low Input Capacitance
- Green Device Available

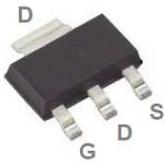
### Typical Applications

- Motor Drive
- Power Tools
- LED Lighting

Package type : SOT-223

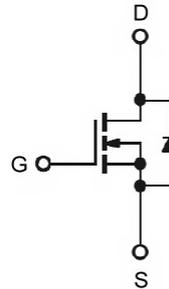
### Packing & Order Information

2,500/Reel

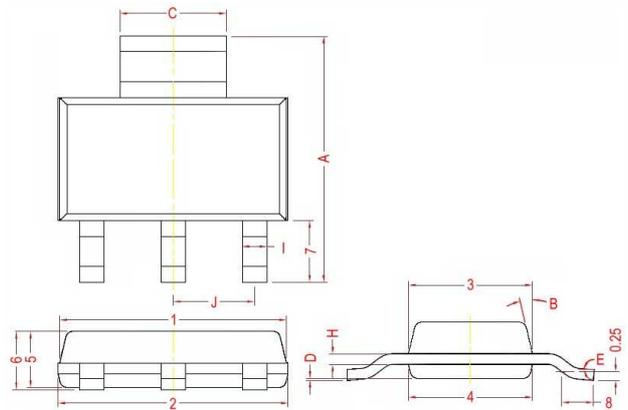


RoHS Compliant

### Graphic Symbol

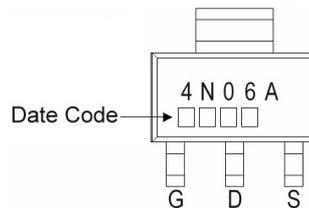


### Package Dimension



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.70	7.30	1	6.30	6.80
C	2.90	3.10	2	6.30	6.80
D	0.02	0.10	3	3.30	3.70
E	0°	10°	4	3.30	3.70
I	0.60	0.80	5	1.40	1.80
H	0.25	0.35	6	1.50	1.80
B	13° Typ.		7	1.55	1.95
J	2.30 Ref.		8	0.80	1.10

### Marking



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#### MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

##### Absolute Maximum Ratings (unless otherwise specified)

Symbol	Parameter	Value	Units
$V_{DS}$	Drain-Source Voltage	60	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current <sup>1</sup> ( $T_A=25^\circ\text{C}$ )	4.0	A
	Continuous Drain Current <sup>1</sup> ( $T_A=70^\circ\text{C}$ )	3.2	A
$I_{DM}$	Pulsed Drain Current <sup>1,2</sup> ( $T_A=25^\circ\text{C}$ )	8	A
$P_D$	Power Dissipation <sup>3</sup> ( $T_A=25^\circ\text{C}$ )	3.1	W
$T_J/T_{STG}$	Operating Junction and Storage Temperature	-55 to +150	$^\circ\text{C}$

##### Thermal Resistance Ratings

Symbol	Parameter	Maximum	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient <sup>1</sup>	40.3	$^\circ\text{C/W}$

##### Electrical Characteristics ( $T_J=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$	1.0	1.8	2.5	V
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$ , $I_D=250\mu\text{A}$	60	-	-	V
$I_{GSS}$	Gate-Source Leakage Current	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 20\text{V}$	-	-	$\pm 100$	nA
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=48\text{V}$ , $V_{GS}=0\text{V}$ , $T_J=25^\circ\text{C}$	-	-	1	$\mu\text{A}$
		$V_{DS}=48\text{V}$ , $V_{GS}=0\text{V}$ , $T_J=55^\circ\text{C}$	-	-	5	$\mu\text{A}$
$R_{DS(on)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10\text{V}$ , $I_D=3\text{A}$	-	85	100	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$ , $I_D=2\text{A}$	-	95	110	$\text{m}\Omega$
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$I_S=1\text{A}$ , $V_{GS}=0\text{V}$ , $T_J=25^\circ\text{C}$	-	0.8	1.0	V
$I_S$	Continuous Source Current <sup>1,4</sup> (Diode)	$V_G=V_D=0\text{V}$ , Force Current	-	-	4	A

#### Notes

1. Surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$ .
3. The power dissipation is limited by  $150^\circ\text{C}$  junction temperature.
4. The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.

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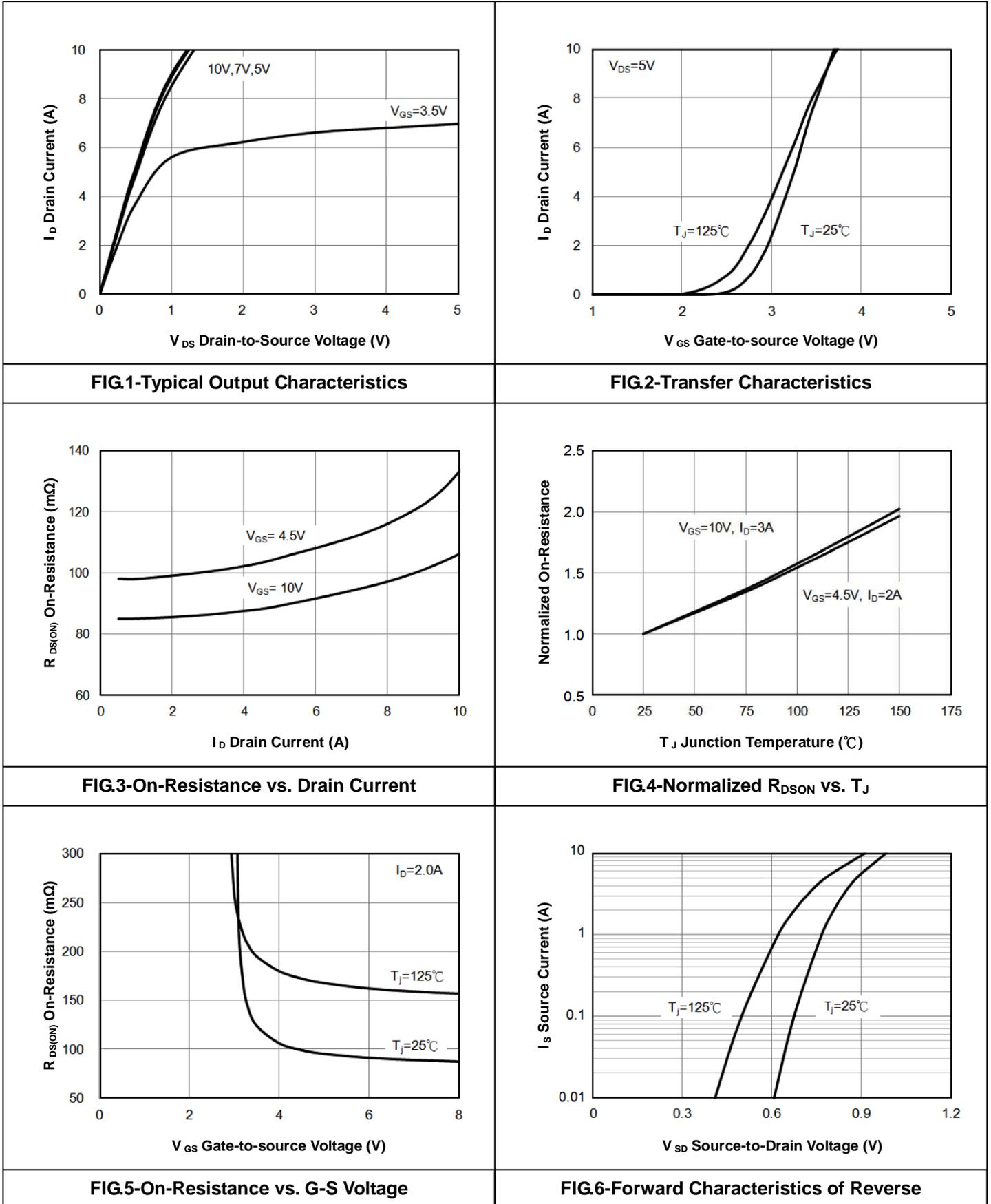
#### Dynamic and switching Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$Q_g$	Total Gate Charge <sup>2</sup>	$V_{DS}=48V$	--	5.1	--	nC
$Q_{gs}$	Gate-Source Charge	$I_D=3A$	--	1.2	--	
$Q_{gd}$	Gate-Drain ("Miller") Charge	$V_{GS}=4.5V$	--	1.9	--	
$t_{d(on)}$	Turn-On Delay Time <sup>2</sup>	$V_{DS}=30V$	--	1.6	--	ns
$t_r$	Rise Time	$I_D=3A$	--	7.3	--	
$t_{d(off)}$	Turn-Off Delay Time	$V_{GS}=10V$	--	25	--	
$t_f$	Fall Time	$R_G=3.3\Omega$	--	14	--	
$C_{ISS}$	Input Capacitance	$V_{DS}=15V$	--	509	--	pF
$C_{OSS}$	Output Capacitance	$V_{GS}=0V$	--	39	--	
$C_{RSS}$	Reverse Transfer Capacitance	$f=1.0MHz$	--	26	--	

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### N-Channel 60-V (D-S) MOSFET

- Typical Electrical Characteristics



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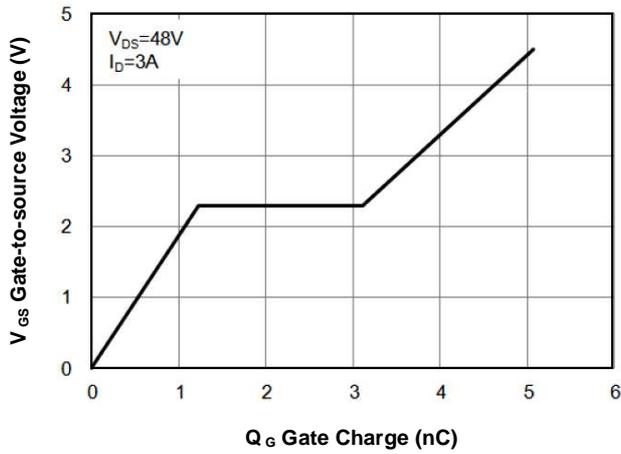


FIG.7-Gate Charge Characteristics

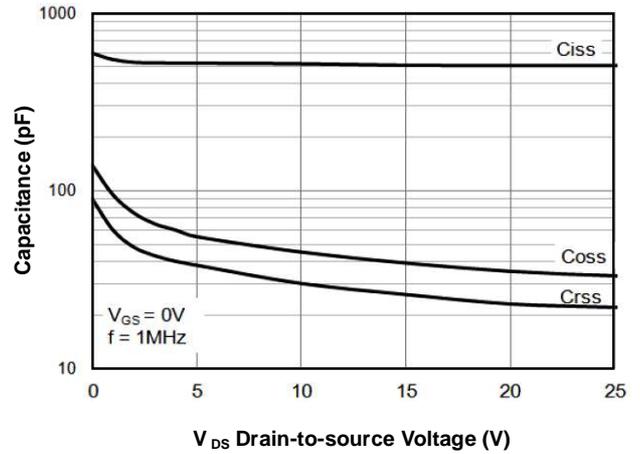


FIG.8-Capacitance Characteristics

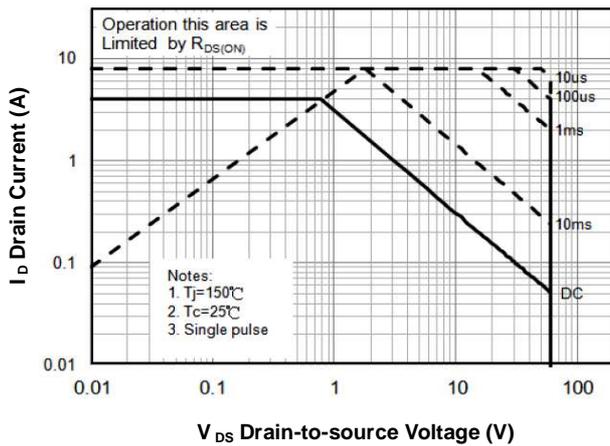


FIG.9-Safe Operating Area

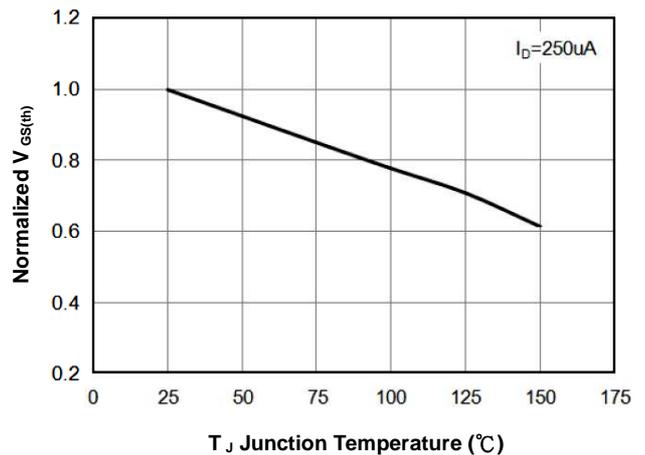


FIG.10-Normalized  $V_{GS(th)}$  vs.  $T_J$

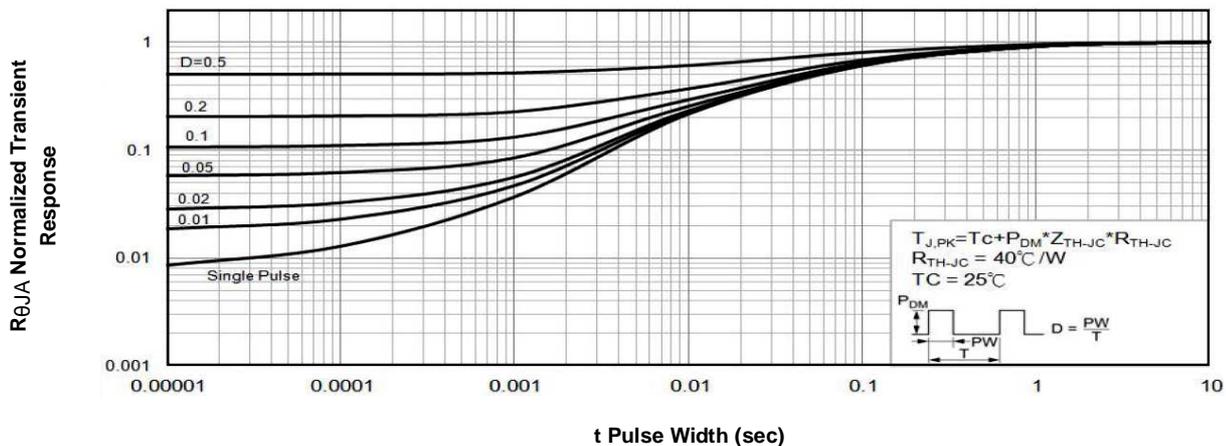


FIG.11-Normalized Maximum Transient Thermal Impedance

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