

MSL60N05

N-Channel 60-V (D-S) MOSFET

Description

The MSL60N05 is a high performance trench N-ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the small power switching and load switch applications.

The device meets the RoHS and Green Product requirement with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Low On-Resistance
- Low Gate Charge
- Low Input Capacitance
- Green Device Available

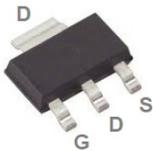
Typical Applications

- Motor Drive
- Power Tools
- LED Lighting

Package type : SOT-223

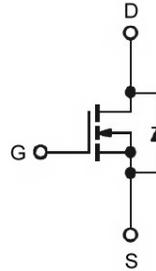
Packing & Order Information

2,500/Reel

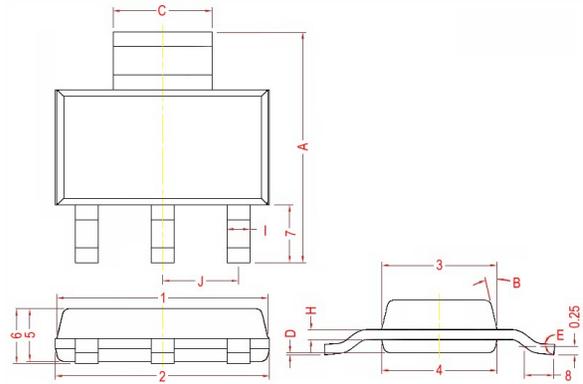


RoHS Compliant

Graphic Symbol

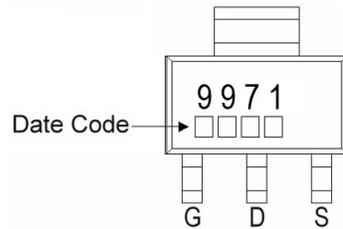


Package Dimension



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.70	7.30	1	6.30	6.80
C	2.90	3.10	2	6.30	6.80
D	0.02	0.10	3	3.30	3.70
E	0°	10°	4	3.30	3.70
I	0.60	0.80	5	1.40	1.80
H	0.25	0.35	6	1.50	1.80
B	13° Typ.		7	1.55	1.95
J	2.30 Ref.		8	0.80	1.10

Marking



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MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (unless otherwise specified)

Symbol	Parameter	Value	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current ¹ ($T_A = 25^\circ\text{C}$)	5	A
	Continuous Drain Current ¹ ($T_A = 70^\circ\text{C}$)	3.5	A
I_{DM}	Pulsed Drain Current ^{1,2} ($T_A = 25^\circ\text{C}$)	30	A
EAS	Single Pulse Avalanche Energy ³	22	mJ
IAS	Single Pulse Avalanche Current ³	21	A
P_D	Power Dissipation ⁴ ($T_A = 25^\circ\text{C}$)	2.7	W
T_J/T_{STG}	Operating Junction and Storage Temperature	-55 to +150	$^\circ\text{C}$

Thermal Resistance Ratings

Symbol	Parameter	Maximum	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ¹	85	$^\circ\text{C/W}$
$R_{\theta JC}$	Maximum Junction-to-case ¹	45	$^\circ\text{C/W}$

Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1.0	-	2.5	V
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	60	-	-	V
I_{GSS}	Gate-Source Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
I_{DSS}	Drain-Source Leakage Current	$V_{DS} = 48\text{V}, V_{GS} = 0\text{V}, T_J = 25^\circ\text{C}$	-	-	1	μA
		$V_{DS} = 48\text{V}, V_{GS} = 0\text{V}, T_J = 55^\circ\text{C}$	-	-	5	μA
$R_{DS(on)}$	Static Drain-Source On-Resistance ²	$V_{GS} = 10\text{V}, I_D = 4\text{A}$	-	-	50	$\text{m}\Omega$
		$V_{GS} = 4.5\text{V}, I_D = 2\text{A}$	-	-	60	$\text{m}\Omega$
V_{SD}	Diode Forward Voltage ²	$I_S = 1\text{A}, V_{GS} = 0\text{V}, T_J = 25^\circ\text{C}$	-	-	1.2	V
I_S	Continuous Source Current ^{1,5} (Diode)	$V_G = V_D = 0\text{V}, \text{Force Current}$	-	-	5	A

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Dynamic and switching Characteristics						
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Q _g	Total Gate Charge ²	V _{DS} =48V	--	19	--	nC
Q _{gs}	Gate-Source Charge	I _D =4A	--	2.6	--	
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =10V	--	4.1	--	
t _{d(on)}	Turn-On Delay Time ²	V _{DS} =30V	--	3	--	ns
t _r	Rise Time	I _D =4A	--	34	--	
t _{d(off)}	Turn-Off Delay Time	V _{GS} =10V	--	23	--	
t _f	Fall Time	R _G =3.3Ω	--	6	--	
C _{ISS}	Input Capacitance	V _{DS} =15V	--	1027	--	pF
C _{OSS}	Output Capacitance	V _{GS} =0V	--	65	--	
C _{RSS}	Reverse Transfer Capacitance	f =1.0MHz	--	46	--	

Notes

1. Surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%.
3. The EAS data shows Max. rating with test condition V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=21A
4. The power dissipation is limited by 150°C junction temperature.
5. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

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- Typical Electrical Characteristics

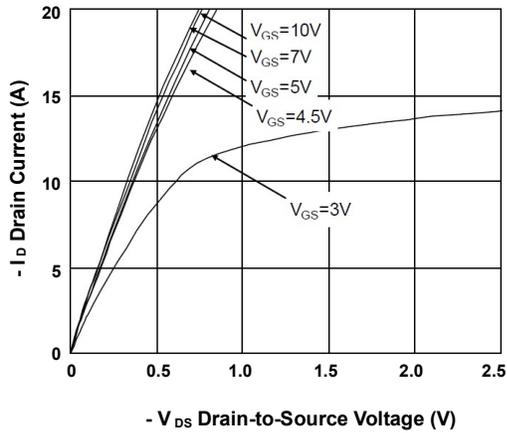


FIG.1-Typical Output Characteristics

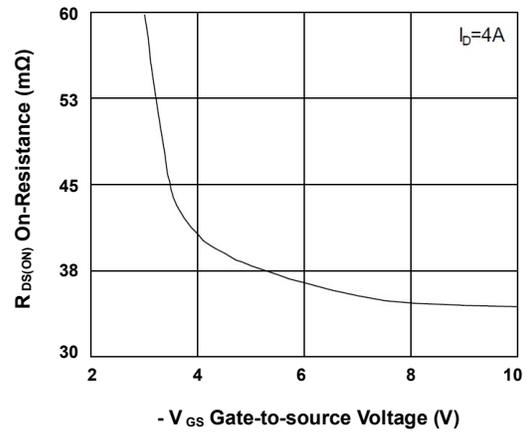


FIG.2-On-Resistance vs. G-S Voltage

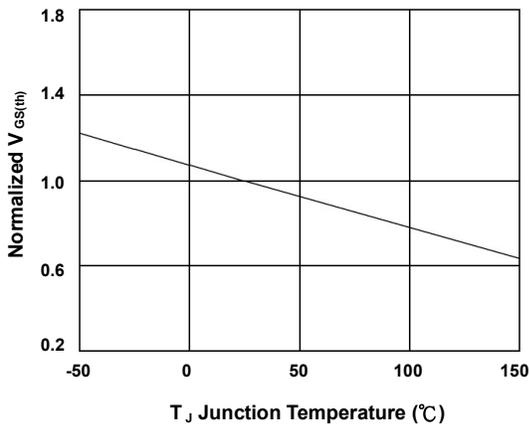


FIG.3-Normalized $V_{GS(th)}$ vs. T_J

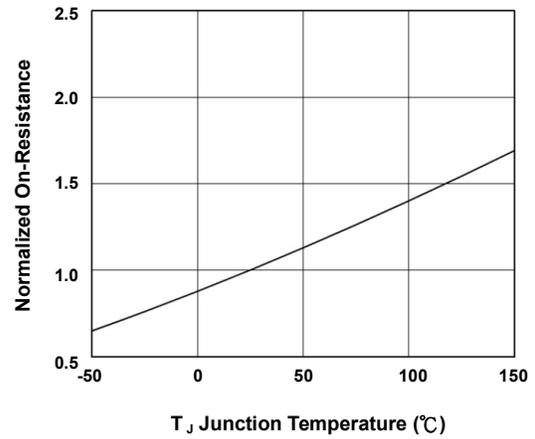


FIG.4-Normalized $R_{DS(on)}$ vs. T_J

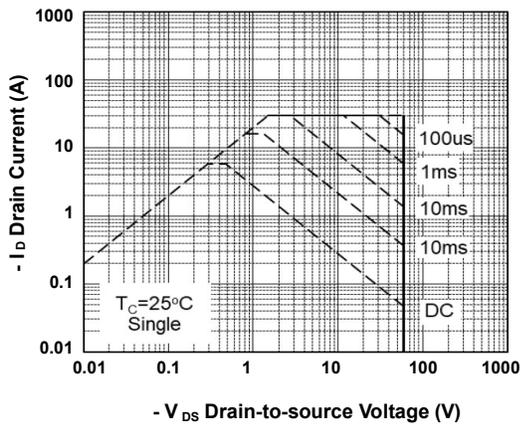


FIG.5-Safe Operating Area

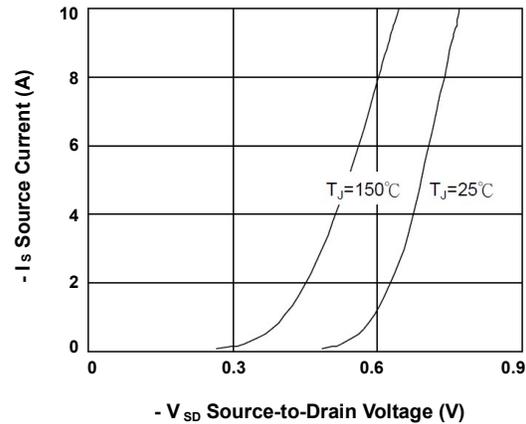


FIG.6-Forward Characteristics of Reverse

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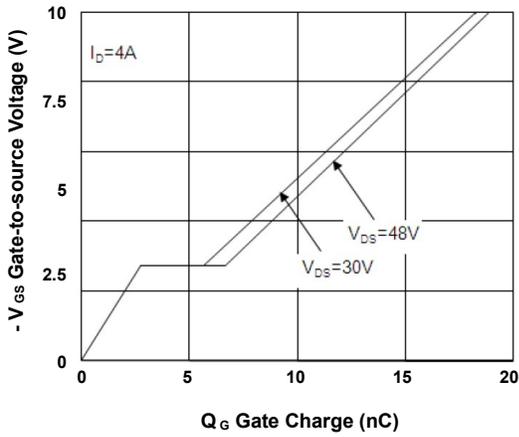


FIG.7-Gate Charge Characteristics

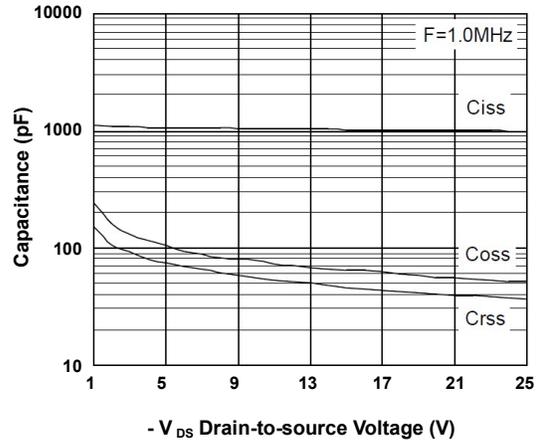


FIG.8-Capacitance Characteristics

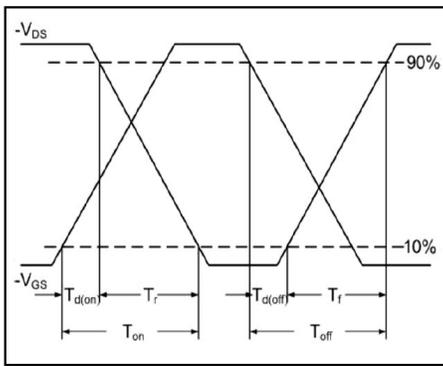


FIG.9-Switching Time Waveform

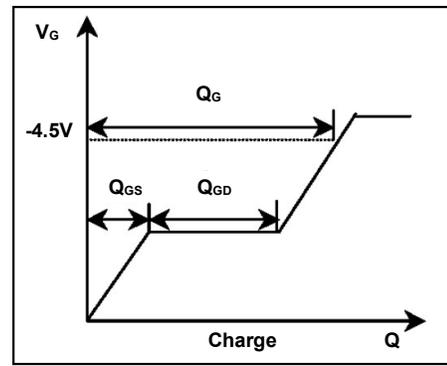


FIG.10-Gate Charge Waveform

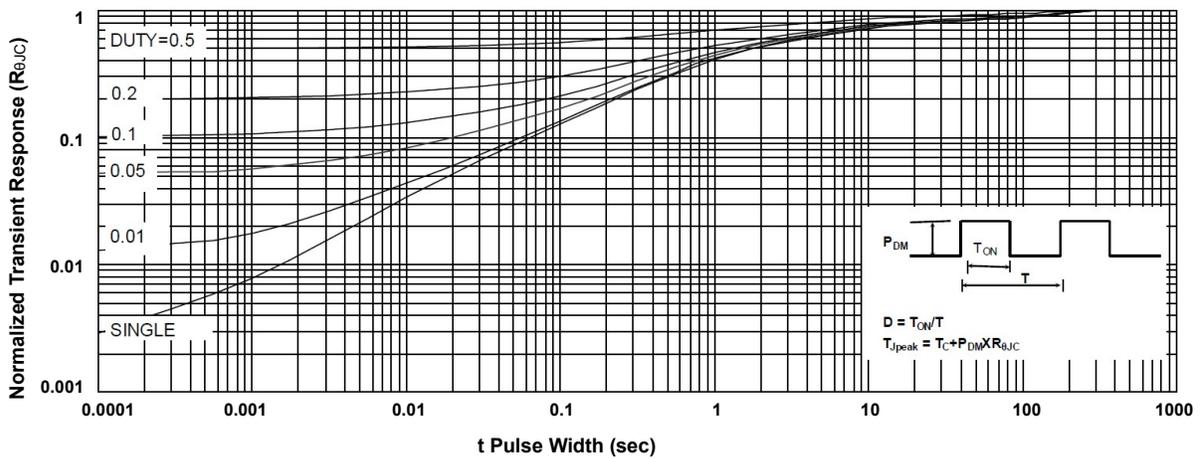


FIG.11-Normalized Maximum Transient Thermal Impedance

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